



# RF Power Field Effect Transistor

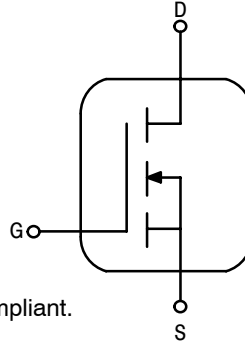
## N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 7.5 volt portable and 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts  
 Output Power — 3 Watts  
 Power Gain — 15 dB  
 Efficiency — 65%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc,  
 520 MHz, 2 dB Overdrive

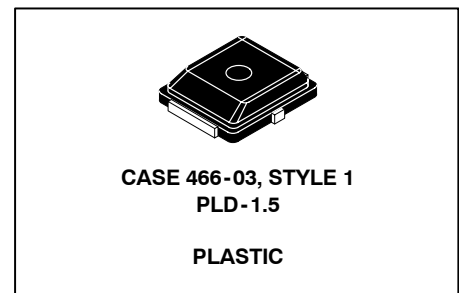
**Features**

- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



**MRF1513NT1**

**520 MHz, 3 W, 12.5 V  
 LATERAL N-CHANNEL  
 BROADBAND  
 RF POWER MOSFET**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-0.5, +40	Vdc
Gate-Source Voltage	V <sub>GS</sub>	±20	Vdc
Drain Current — Continuous	I <sub>D</sub>	2	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C (1) Derate above 25°C	P <sub>D</sub>	31.25 0.25	W W/°C
Storage Temperature Range	T <sub>stg</sub>	- 65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	150	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	4	°C/W

**Table 3. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

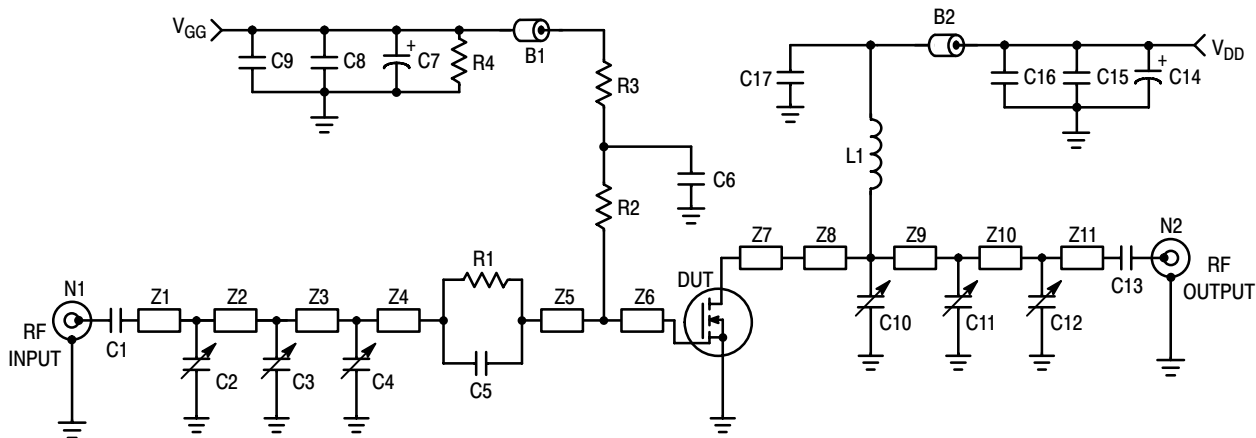
1. Calculated based on the formula  $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

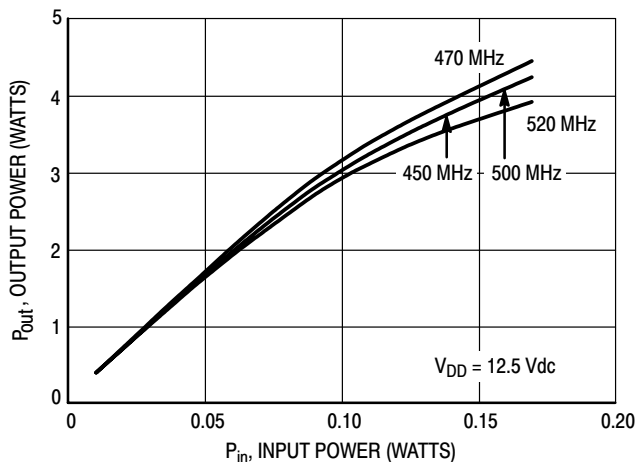
Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Zero Gate Voltage Drain Current ( $V_{DS} = 40\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 10\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 12.5\text{ Vdc}$ , $I_D = 60\ \mu\text{A}$ )	$V_{GS(th)}$	1	1.7	2.1	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 500\text{ mAdc}$ )	$V_{DS(on)}$	—	0.65	—	Vdc
<b>Dynamic Characteristics</b>					
Input Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{iss}$	—	33	—	pF
Output Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{oss}$	—	16.5	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{rss}$	—	2.2	—	pF
<b>Functional Tests</b> (In Freescale Test Fixture)					
Common-Source Amplifier Power Gain ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 3\text{ Watts}$ , $I_{DQ} = 50\text{ mA}$ , $f = 520\text{ MHz}$ )	$G_{ps}$	—	15	—	dB
Drain Efficiency ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 3\text{ Watts}$ , $I_{DQ} = 50\text{ mA}$ , $f = 520\text{ MHz}$ )	$\eta$	—	65	—	%



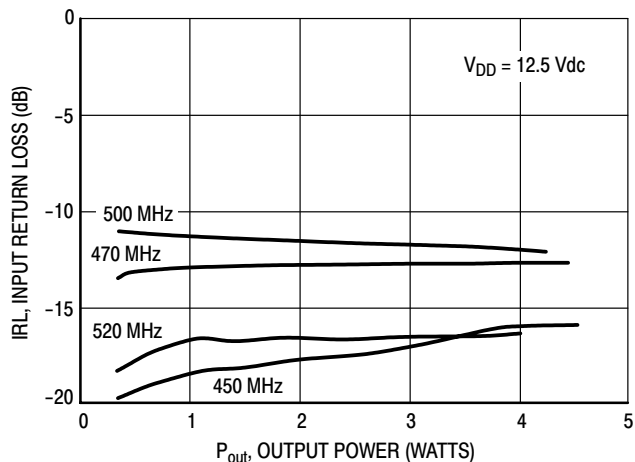
B1, B2	Short Ferrite Beads, Fair Rite Products #2743021446	R4	33 k $\Omega$ , 1/8 W Resistor
C1, C13	240 pF, 100 mil Chip Capacitors	Z1	0.236" x 0.080" Microstrip
C2, C3, C4, C10,	0 to 20 pF Trimmer Capacitors	Z2	0.981" x 0.080" Microstrip
C11, C12	10 $\mu$ F, 50 V Electrolytic Capacitors	Z3	0.240" x 0.080" Microstrip
C5, C6, C17	120 pF, 100 mil Chip Capacitors	Z4	0.098" x 0.080" Microstrip
C7, C14	10 $\mu$ F, 50 V Electrolytic Capacitors	Z5	0.192" x 0.080" Microstrip
C8, C15	1,200 pF, 100 mil Chip Capacitors	Z6, Z7	0.260" x 0.223" Microstrip
C9, C16	0.1 $\mu$ F, 100 mil Chip Capacitors	Z8	0.705" x 0.080" Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z9	0.342" x 0.080" Microstrip
N1, N2	Type N Flange Mounts	Z10	0.347" x 0.080" Microstrip
R1, R3	15 $\Omega$ Chip Resistors (0805)	Z11	0.846" x 0.080" Microstrip
R2	1 k $\Omega$ , 1/8 W Resistor	Board	Glass Teflon <sup>®</sup> , 31 mils, 2 oz. Copper

**Figure 1. 450 - 520 MHz Broadband Test Circuit**

### TYPICAL CHARACTERISTICS, 450 - 520 MHz



**Figure 2. Output Power versus Input Power**



**Figure 3. Input Return Loss versus Output Power**

## TYPICAL CHARACTERISTICS, 450 - 520 MHz

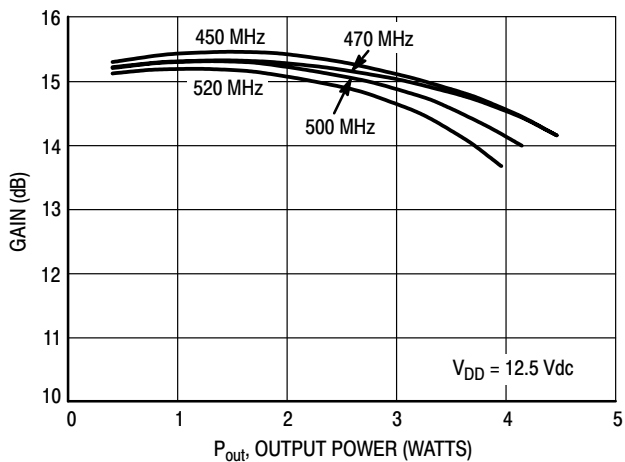


Figure 4. Gain versus Output Power

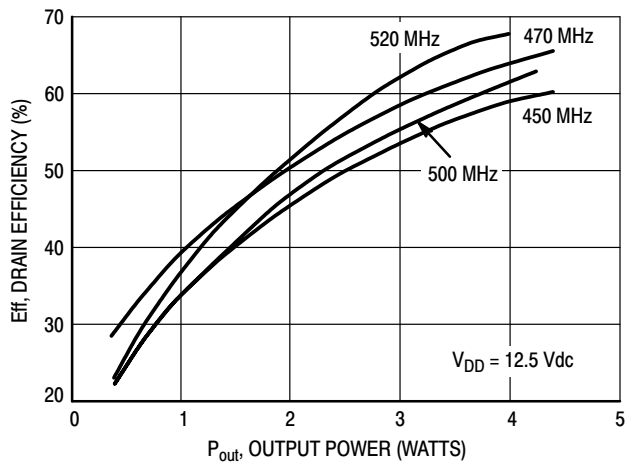


Figure 5. Drain Efficiency versus Output Power

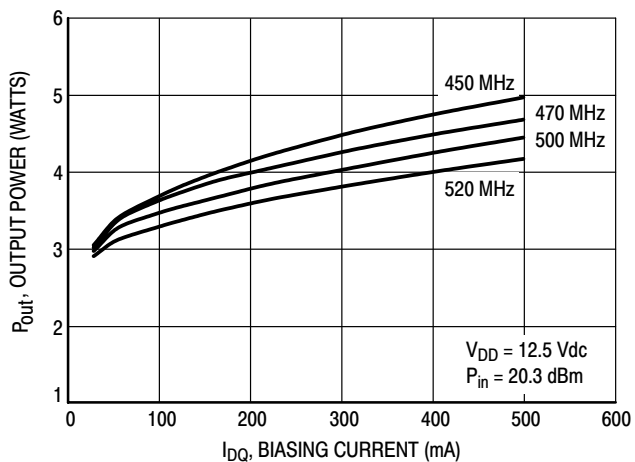


Figure 6. Output Power versus Biasing Current

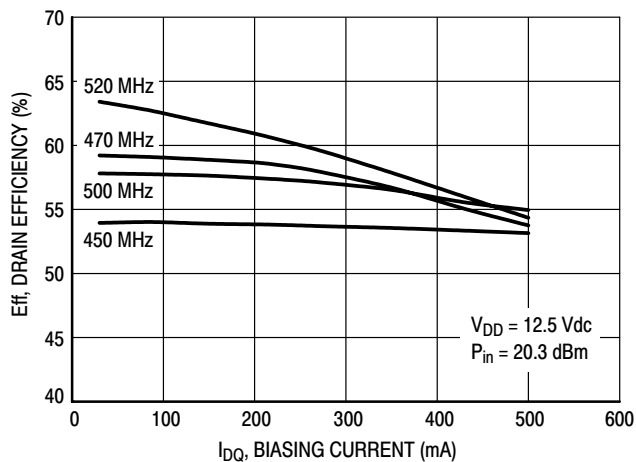


Figure 7. Drain Efficiency versus Biasing Current

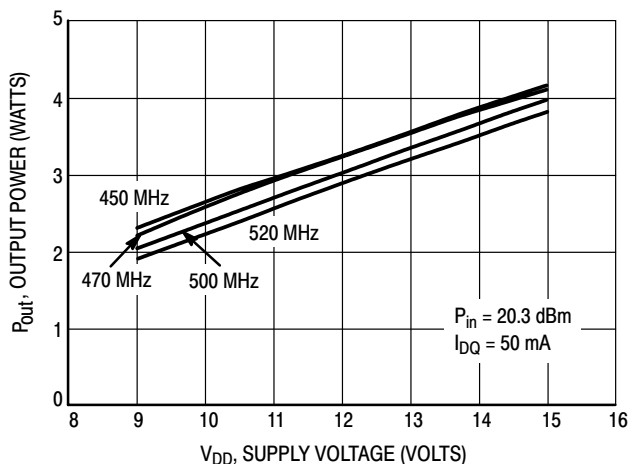


Figure 8. Output Power versus Supply Voltage

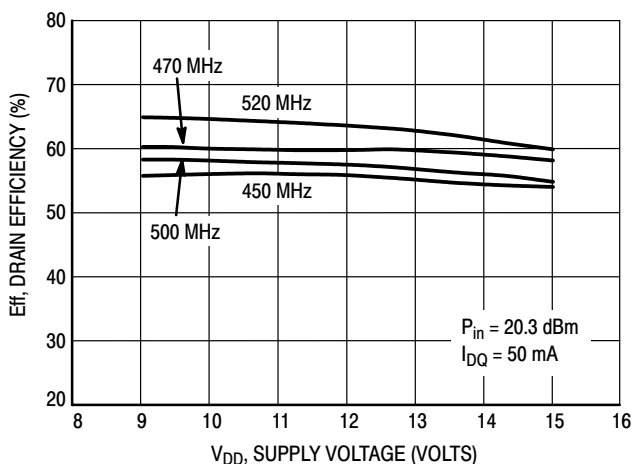
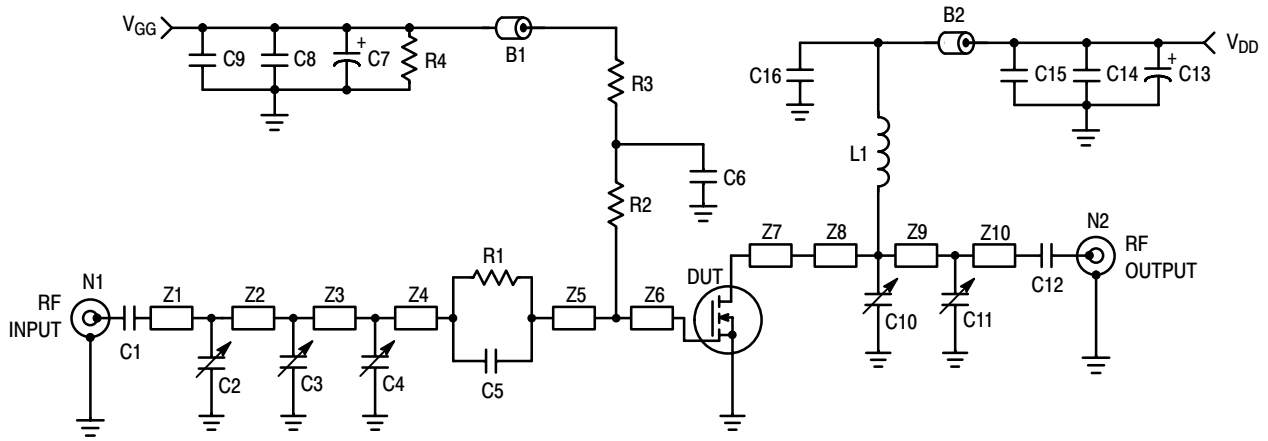


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products #2743021446	R3	15 $\Omega$ Chip Resistor (0805)
C1, C12	330 pF, 100 mil Chip Capacitors	R4	33 k $\Omega$ , 1/8 W Resistor
C2, C3, C4,		Z1	0.253" x 0.080" Microstrip
C10, C11	1 to 20 pF Trimmer Capacitors	Z2	0.958" x 0.080" Microstrip
C5, C6, C16	120 pF, 100 mil Chip Capacitors	Z3	0.247" x 0.080" Microstrip
C7, C13	10 $\mu$ F, 50 V Electrolytic Capacitors	Z4	0.193" x 0.080" Microstrip
C8, C14	1,200 pF, 100 mil Chip Capacitors	Z5	0.132" x 0.080" Microstrip
C9, C15	0.1 $\mu$ F, 100 mil Chip Capacitors	Z6, Z7	0.260" x 0.223" Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z8	0.494" x 0.080" Microstrip
N1, N2	Type N Flange Mounts	Z9	0.941" x 0.080" Microstrip
R1	15 $\Omega$ Chip Resistor (0805)	Z10	0.452" x 0.080" Microstrip
R2	1 k $\Omega$ , 1/8 W Resistor	Board	Glass Teflon <sup>®</sup> , 31 mils, 2 oz. Copper

Figure 10. 400 - 470 MHz Broadband Test Circuit

### TYPICAL CHARACTERISTICS, 400 - 470 MHz

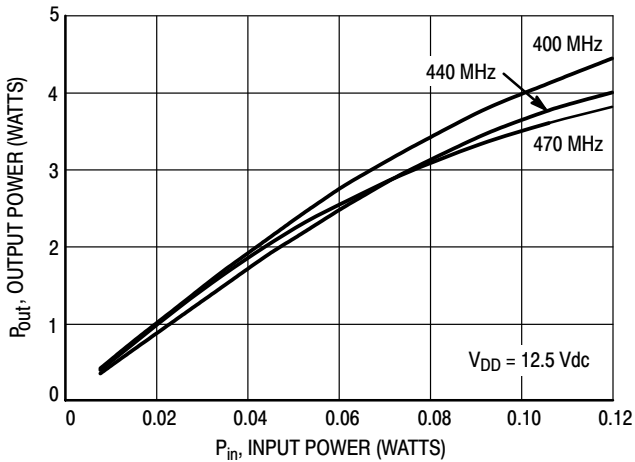


Figure 11. Output Power versus Input Power

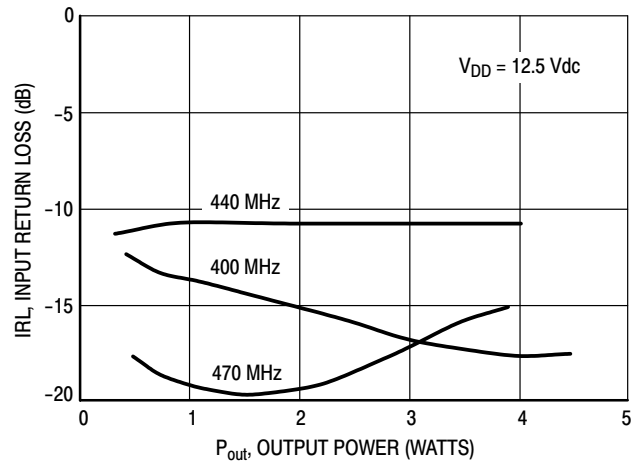


Figure 12. Input Return Loss versus Output Power

## TYPICAL CHARACTERISTICS, 400 - 470 MHz

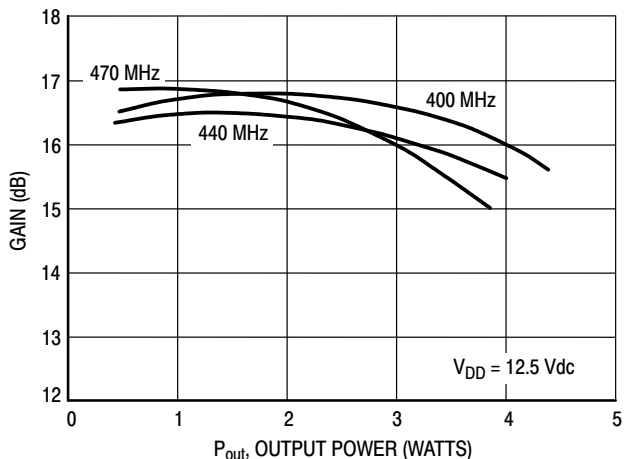


Figure 13. Gain versus Output Power

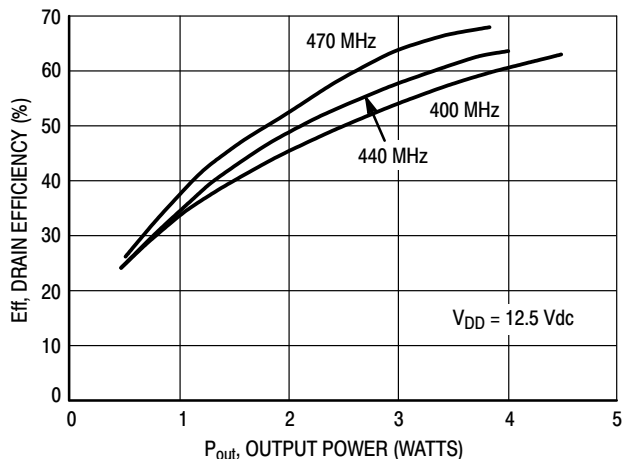


Figure 14. Drain Efficiency versus Output Power

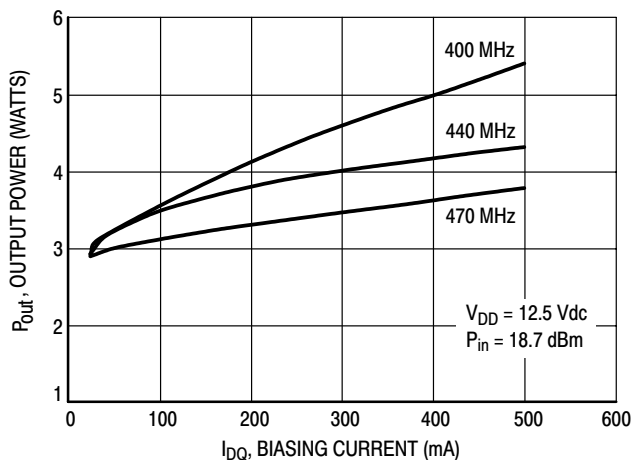


Figure 15. Output Power versus Biasing Current

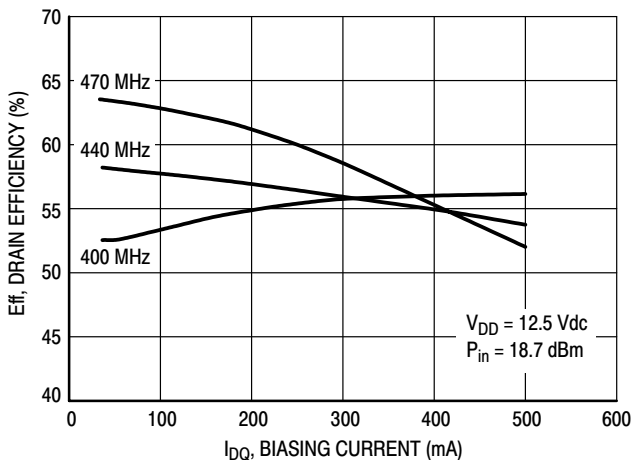


Figure 16. Drain Efficiency versus Biasing Current

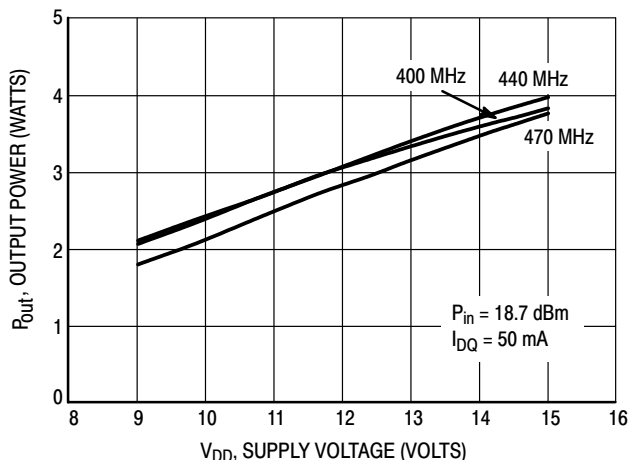


Figure 17. Output Power versus Supply Voltage

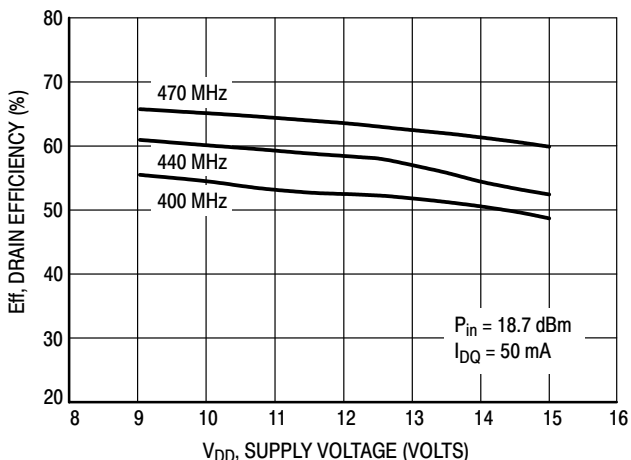
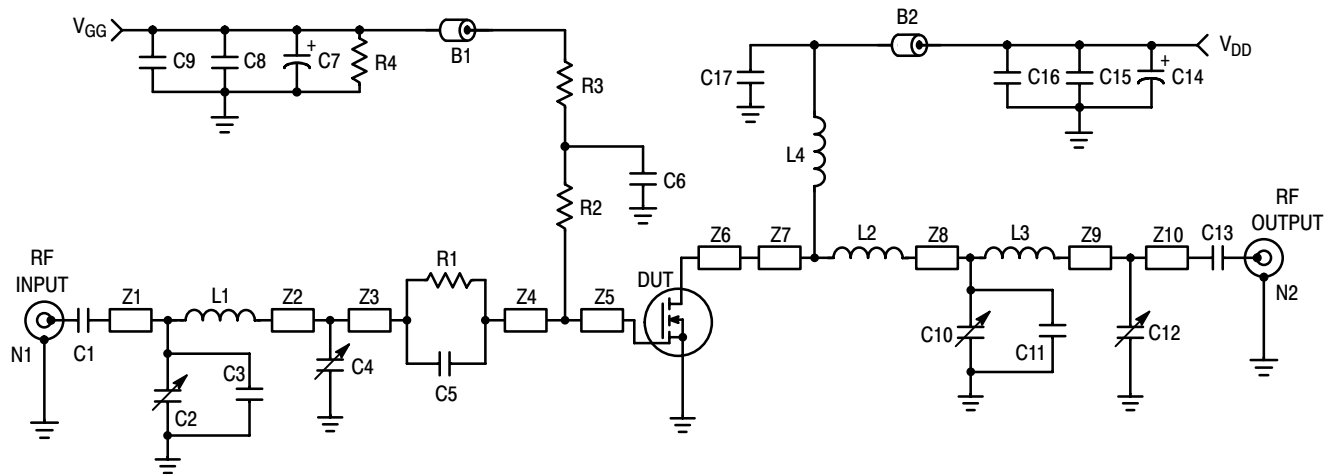


Figure 18. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Beads, Fair Rite Products #2743021446	L4	33 nH, 5 Turn, Coilcraft
C1, C13	330 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C2, C4, C10, C12	0 to 20 pF Trimmer Capacitors	R1	15 $\Omega$ Chip Resistor (0805)
C3	12 pF, 100 mil Chip Capacitor	R2	56 $\Omega$ , 1/8 W Chip Resistor
C5	130 pF, 100 mil Chip Capacitor	R3	10 $\Omega$ , 1/8 W Chip Resistor
C6, C17	120 pF, 100 mil Chip Capacitors	R4	33 k $\Omega$ , 1/8 W Chip Resistor
C7, C14	10 $\mu$ F, 50 V Electrolytic Capacitors	Z1	0.115" x 0.080" Microstrip
C8, C15	1,000 pF, 100 mil Chip Capacitors	Z2	0.230" x 0.080" Microstrip
C9, C16	0.1 $\mu$ F, 100 mil Chip Capacitors	Z3	1.034" x 0.080" Microstrip
C11	18 pF, 100 mil Chip Capacitor	Z4	0.202" x 0.080" Microstrip
L1	26 nH, 4 Turn, Coilcraft	Z5, Z6	0.260" x 0.223" Microstrip
L2	8 nH, 3 Turn, Coilcraft	Z7	1.088" x 0.080" Microstrip
L3	55.5 nH, 5 Turn, Coilcraft	Z8	0.149" x 0.080" Microstrip
		Z9	0.171" x 0.080" Microstrip
		Z10	0.095" x 0.080" Microstrip
		Board	Glass Teflon <sup>®</sup> , 31 mils, 2 oz. Copper

Figure 19. 135 - 175 MHz Broadband Test Circuit

### TYPICAL CHARACTERISTICS, 135 - 175 MHz

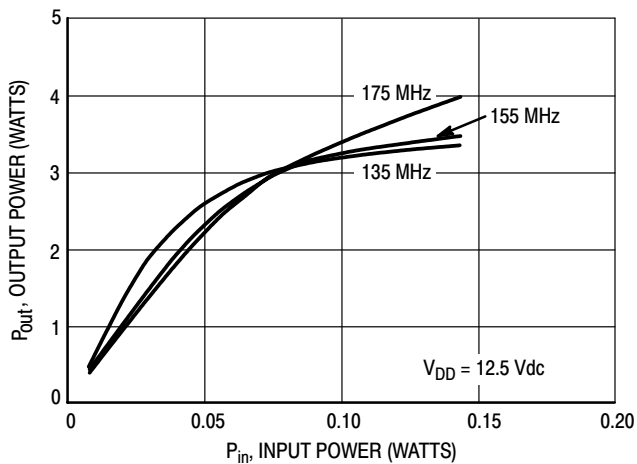


Figure 20. Output Power versus Input Power

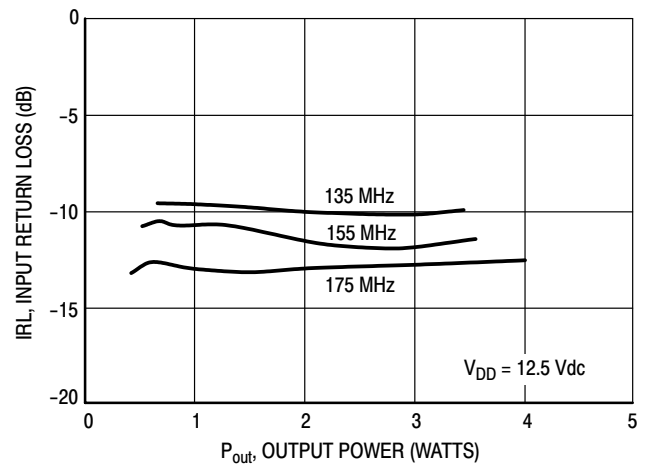


Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 - 175 MHz

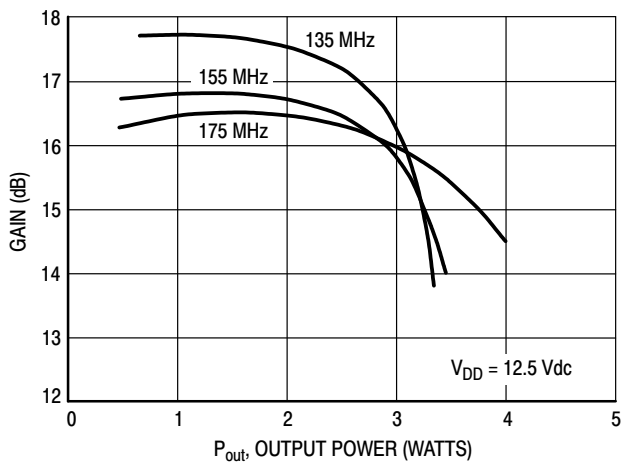


Figure 22. Gain versus Output Power

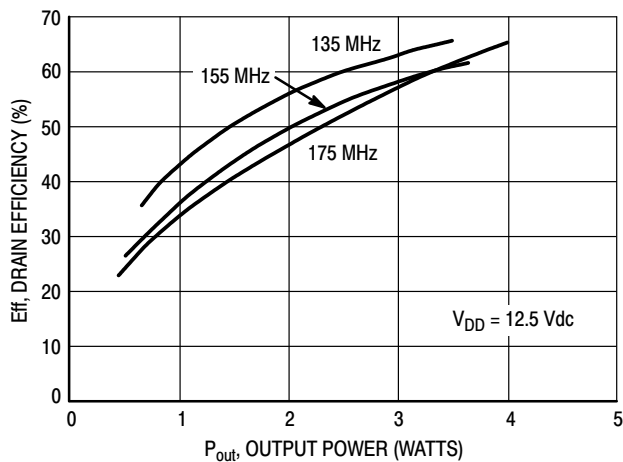


Figure 23. Drain Efficiency versus Output Power

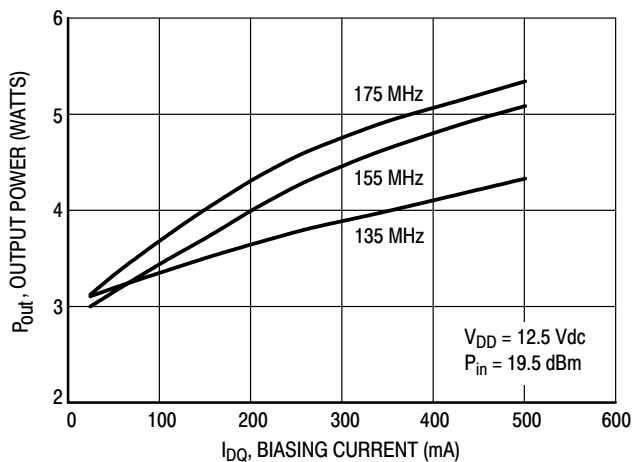


Figure 24. Output Power versus Biasing Current

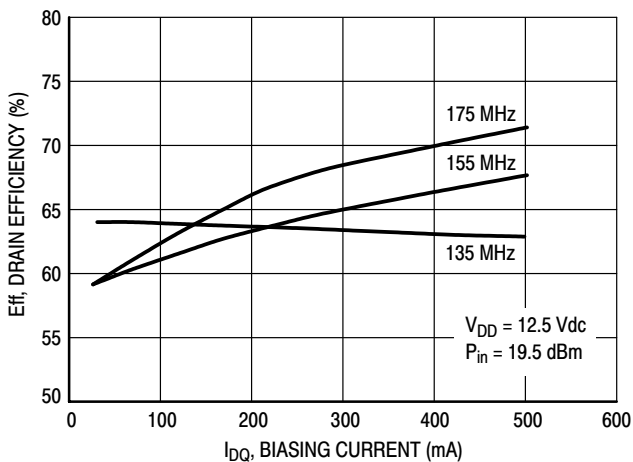


Figure 25. Drain Efficiency versus Biasing Current

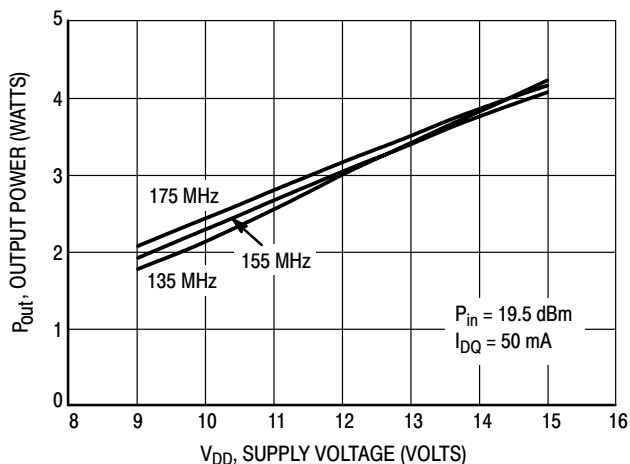


Figure 26. Output Power versus Supply Voltage

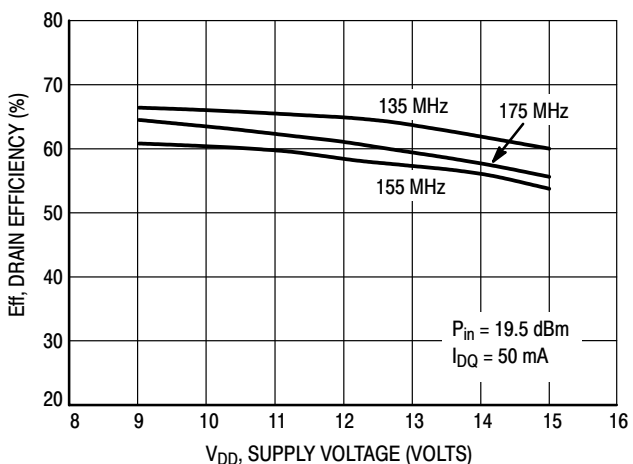
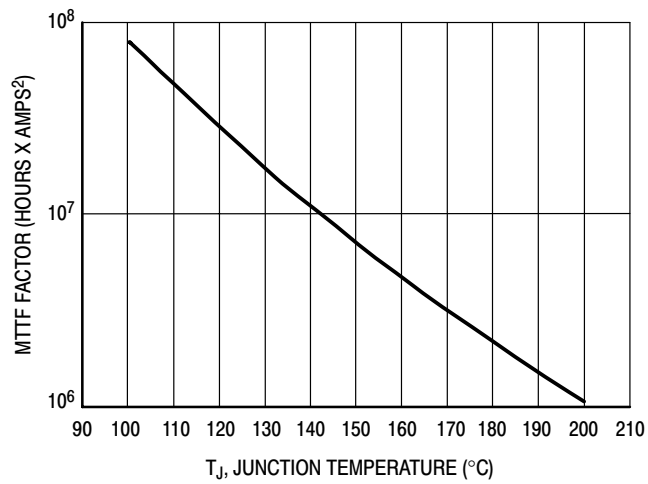


Figure 27. Drain Efficiency versus Supply Voltage

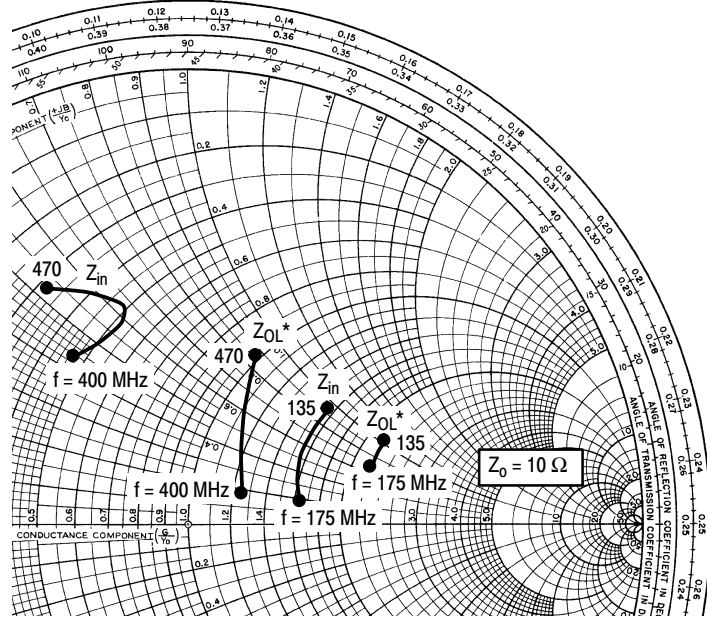
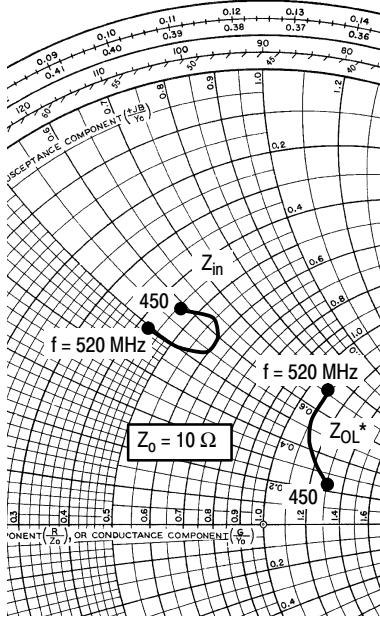


## TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 28. MTTF Factor versus Junction Temperature**



$V_{DD} = 12.5 \text{ V}$ ,  $I_{DQ} = 50 \text{ mA}$ ,  $P_{out} = 3 \text{ W}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
450	4.64 +j5.82	13.11 +j2.15
470	5.42 +j6.34	12.16 +j3.26
500	5.96 +j5.45	11.03 +j5.42
520	4.28 +j4.94	10.99 +j7.18

$V_{DD} = 12.5 \text{ V}$ ,  $I_{DQ} = 50 \text{ mA}$ ,  $P_{out} = 3 \text{ W}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
400	4.72 +j4.38	12.57 +j1.88
440	4.88 +j6.34	11.21 +j5.87
470	3.22 +j5.24	9.82 +j8.63

$V_{DD} = 12.5 \text{ V}$ ,  $I_{DQ} = 50 \text{ mA}$ ,  $P_{out} = 3 \text{ W}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
135	16.55 +j1.82	22.01 +j10.32
155	15.59 +j5.38	22.03 +j8.07
175	15.55 +j9.43	22.08 +j6.85

$Z_{in}$  = Complex conjugate of source impedance with parallel 15  $\Omega$  resistor and 120 pF capacitor in series with gate. (See Figure 1).

$Z_{OL}^*$  = Complex conjugate of the load impedance at given output power, voltage, frequency, and  $\eta_D > 50\%$ .

$Z_{in}$  = Complex conjugate of source impedance with parallel 15  $\Omega$  resistor and 130 pF capacitor in series with gate. (See Figure 10).

$Z_{OL}^*$  = Complex conjugate of the load impedance at given output power, voltage, frequency, and  $\eta_D > 50\%$ .

$Z_{in}$  = Complex conjugate of source impedance with parallel 15  $\Omega$  resistor and 130 pF capacitor in series with gate. (See Figure 19).

$Z_{OL}^*$  = Complex conjugate of the load impedance at given output power, voltage, frequency, and  $\eta_D > 50\%$ .

Note:  $Z_{OL}^*$  was chosen based on tradeoffs between gain, drain efficiency, and device stability.

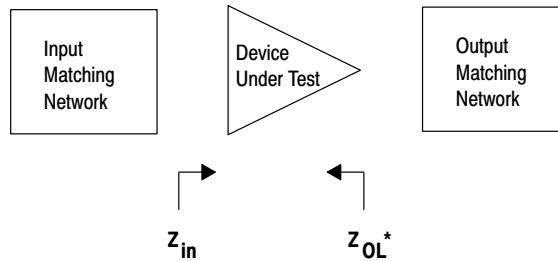


Figure 29. Series Equivalent Input and Output Impedance

**Table 5. Common Source Scattering Parameters ( $V_{DD} = 12.5$  Vdc)**

$I_{DQ} = 50$  mA

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
50	0.93	-94	22.09	125	0.044	33	0.77	-81
100	0.81	-131	12.78	101	0.052	6	0.61	-115
200	0.76	-153	6.31	81	0.047	-10	0.59	-135
300	0.76	-160	3.92	69	0.044	-19	0.64	-142
400	0.77	-164	2.74	60	0.040	-26	0.70	-147
500	0.79	-167	1.99	54	0.036	-31	0.75	-151
600	0.80	-169	1.55	48	0.034	-37	0.80	-155
700	0.81	-171	1.25	44	0.028	-40	0.82	-158
800	0.82	-172	1.02	38	0.027	-42	0.86	-161
900	0.83	-173	0.85	35	0.017	-42	0.88	-163
1000	0.84	-175	0.70	29	0.018	-49	0.91	-166

$I_{DQ} = 500$  mA

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
50	0.84	-127	32.57	112	0.025	17	0.64	-130
100	0.80	-152	17.23	97	0.025	13	0.64	-153
200	0.78	-166	8.62	85	0.025	-9	0.65	-163
300	0.78	-171	5.58	79	0.023	-9	0.67	-166
400	0.78	-173	4.08	72	0.022	-9	0.69	-166
500	0.78	-175	3.14	68	0.020	-10	0.71	-167
600	0.79	-176	2.55	63	0.022	-15	0.74	-168
700	0.79	-177	2.14	60	0.019	-20	0.76	-168
800	0.80	-178	1.80	54	0.018	-31	0.79	-170
900	0.81	-178	1.54	51	0.015	-25	0.80	-170
1000	0.82	-179	1.31	46	0.012	-36	0.81	-172

$I_{DQ} = 1$  A

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
50	0.84	-129	32.57	111	0.023	24	0.61	-137
100	0.80	-153	17.04	97	0.024	13	0.64	-156
200	0.78	-167	8.52	85	0.023	5	0.65	-165
300	0.77	-172	5.53	79	0.020	-7	0.67	-167
400	0.77	-174	4.06	73	0.020	-11	0.69	-167
500	0.78	-175	3.13	69	0.021	-9	0.72	-167
600	0.78	-177	2.54	64	0.017	-26	0.74	-168
700	0.78	-177	2.13	60	0.017	-14	0.75	-168
800	0.79	-178	1.81	55	0.015	-23	0.78	-170
900	0.80	-178	1.54	51	0.013	-31	0.79	-170
1000	0.80	-179	1.30	46	0.011	-17	0.80	-172

## APPLICATIONS INFORMATION

### DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Freescale Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

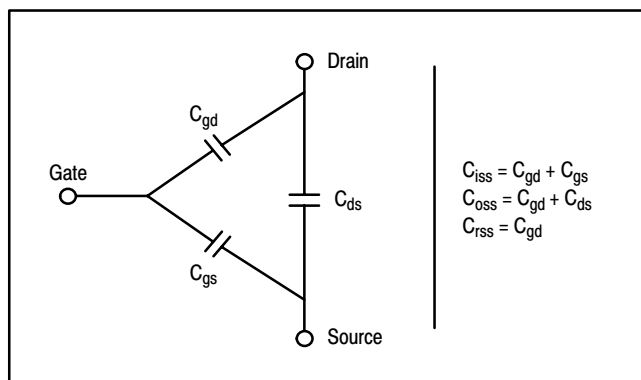
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ). These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



### DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $R_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed  $V_{DS(on)}$ . For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

$BV_{DSS}$  values for this device are higher than normally required for typical applications. Measurement of  $BV_{DSS}$  is not recommended and may result in possible damage to the device.

### GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high - on the order of  $10^9 \Omega$  — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

### DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current ( $I_{DQ}$ ), whose value is application dependent. This device was characterized at  $I_{DQ} = 50 \text{ mA}$ , which is the suggested value of bias current for typical applications. For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

### GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

## **MOUNTING**

The specified maximum thermal resistance of 4°C/W assumes a majority of the 0.065" x 0.180" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Freescale Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package" for additional information.

## **AMPLIFIER DESIGN**

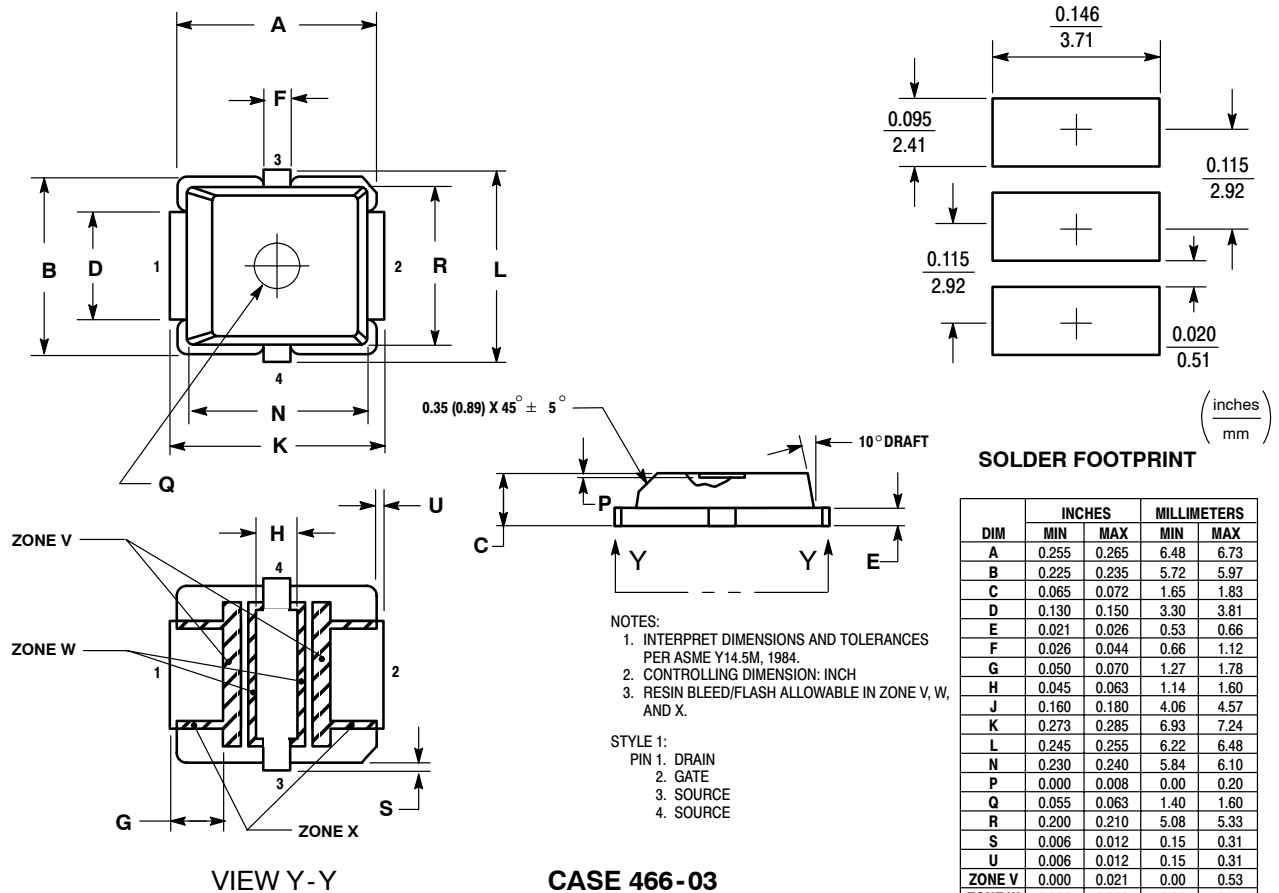
Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Freescale Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal impedances are provided, and will yield a good

first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Freescale Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

## PACKAGE DIMENSIONS



## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN211A: Field Effect Transistors in Theory and Practice
- AN215A: RF Small-Signal Design Using Two-Port Parameters
- AN721: Impedance Matching Networks Applied to RF Power Transistors
- AN4005: Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
10	Feb. 2008	<ul style="list-style-type: none"><li>• Changed DC Bias <math>I_{DQ}</math> value from 150 to 50 to match Functional Test <math>I_{DQ}</math> specification, p. 12</li><li>• Added Product Documentation and Revision History, p. 15</li></ul>
11	June 2008	<ul style="list-style-type: none"><li>• Corrected specified performance values for power gain and efficiency on p. 1 to match typical performance values in the functional test table on p. 2</li></ul>

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or +1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2008. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

